A Multi-perspective approach to IC power grid development for 7nm based designs

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Abstract

- IC Power delivery network is designed to provide required voltage to the cells performing logic operation. With advanced technology scaling there is increase in power density and metal wire resistances, causing higher IR drop. This can result in functional failures. Power grid impacts available routing resources, design rule violations and related layout cleanup effort, signal loading and power consumption.

- While the chip designers have focused on aspects of SoC design, there is very less exploration on how the power grid impacts multiple design aspects.

- This work focuses on highlighting aspects impacted by the power grid design.

Outline

- Motivation
- Design of Experiments
- PG Grid Evaluations
- Analysis Results
- Conclusion

Motivation

Problem statement –

- Increased power density and stringent technology manufacturing rules has made power grid design complex and challenging.
- Traditional approach is based on only improving voltage levels.
- It is very important to understand impact of power grid on different design aspects.

Motivation -

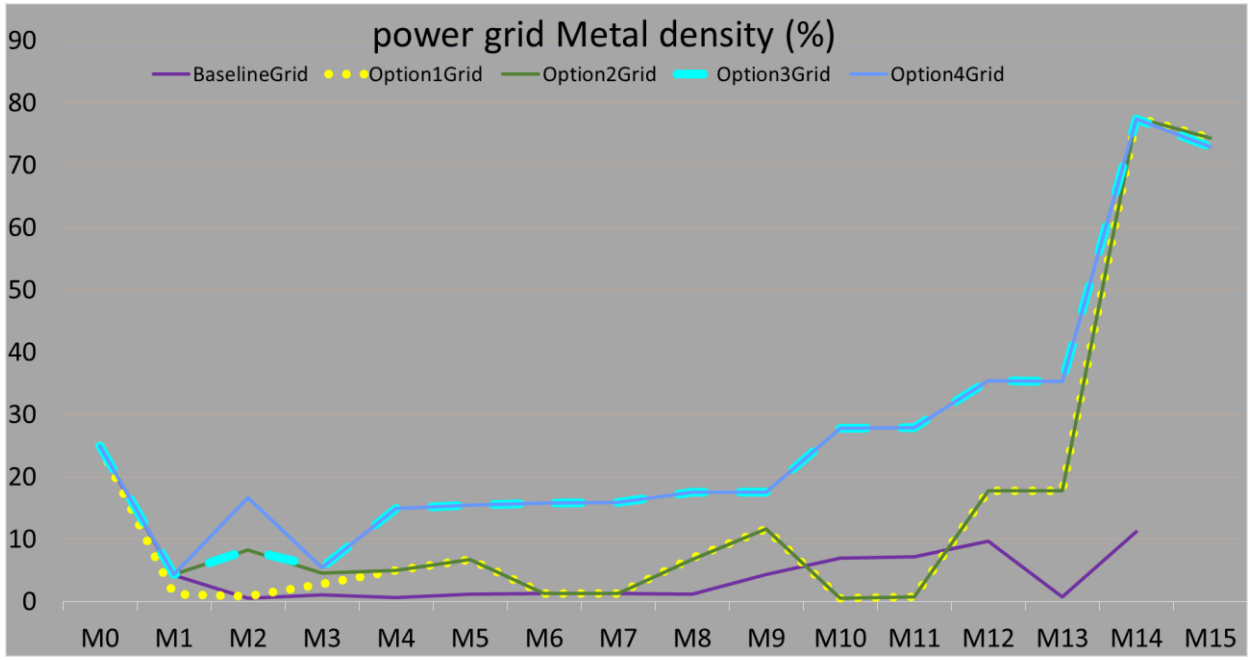
- Study impact of power grid design on multiple design aspects and provide methodology framework for optimal 7nm power grid design considering different design aspects.

Power grid evaluations

Five PG grid options were chosen for evaluations – these options were derived considering

- TSMC™ N7 Standard cell architecture which puts restriction M1 PG pitch –target to reduce M1 tapping distance
- Local power grid layer selection – standard cell pin accessibility versus charge sharing
- Routing resource effectiveness of via pillared grid versus continuous grid
- Grid with lower impedance path to voltage sources (bumps) as well as to the decap network
- An overdesigned grid to assess impact on routability, power dissipation and run times

Baseline option	Option-1	Option-2	Option-3	Option-4
- Dual M1 continuous with same-net pitch X um - VIA pilar on all layers from M2 to M8	-VIA pillar on M1, M2, M6, M7, M11 and M12 - M1 same net pitch @ X/2 um by assigning power and ground on dual M1	- Same as Option1 except M1/M2 continuous grid and M3 pitch reduced	continuous grid on all layers - Slight reduction of M3 pitch	- Doubled M2 PG metal density than in option3 - continuous grid on all layers

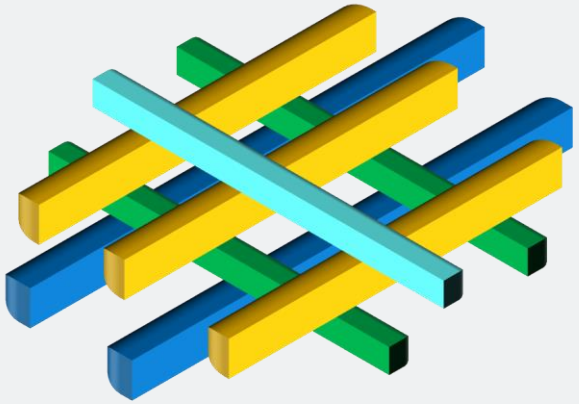


PG Grid Evaluations - Baseline Option

Baseline option Strategy :
- Based on sample power grid from foundry
- Via pillar grid with via pillars (staples) on all layer between M9 and M1
- M13 layer is also staple layer

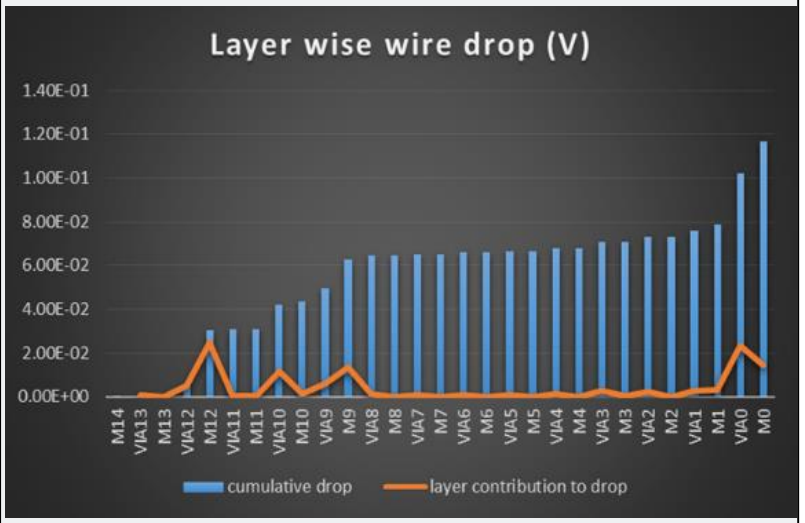
Via pillar – intermediate layers are used only for via overhangs – no continuous wires on particular layers

Via pillar



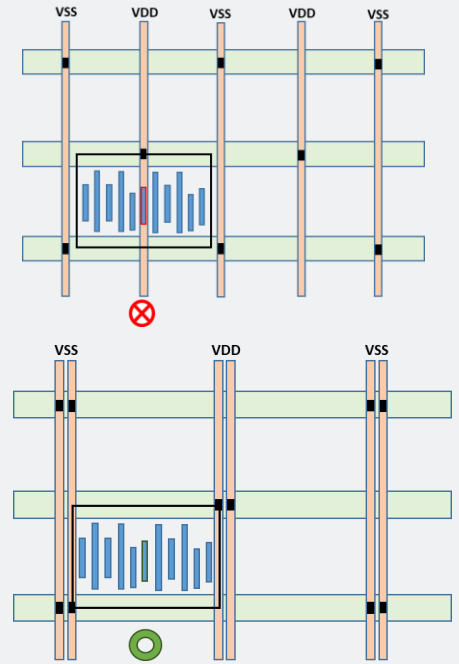
IR drop analysis summary

Parameters	Baseline option
IR drop analysis Runs	
Average Power (mW)	354.14
Worst Static IR drop (% of Nom voltage)	4.48
IR drop violation count (threshold 3%)	269
Worst Dynamic IR (% of Nom voltage)	15.60
Dynamic IR violation count (thres. -10%)	4657
PG decap (pF)	4.552



Major IR drop – M12, VIA0 and M0

TSMC™ N7 - 7nm standard cell library [1]
- is designed to allow better standard cell placement freedom by making two M1 straps closer

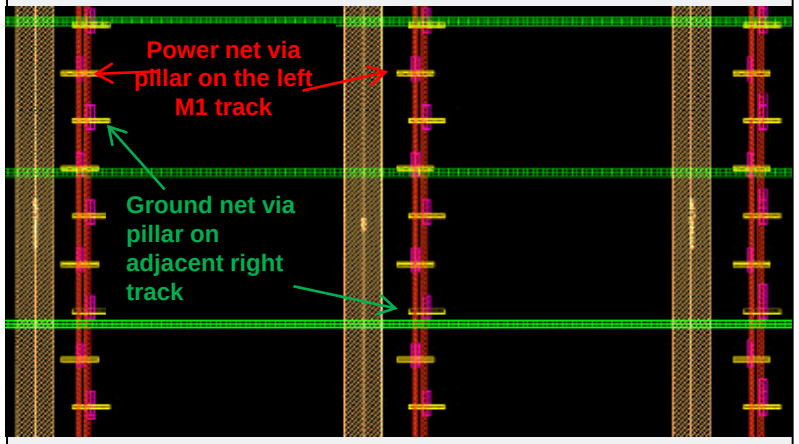


- For big cells, minimum 2 adjacent M1 tracks are reserved for M1 PG feed-through.
- Limits dual M1 PG net pitch reduction – causing high IR drop on M0 (~2%)

PG Grid Evaluations - Option1 Grid

Option1 Strategy :

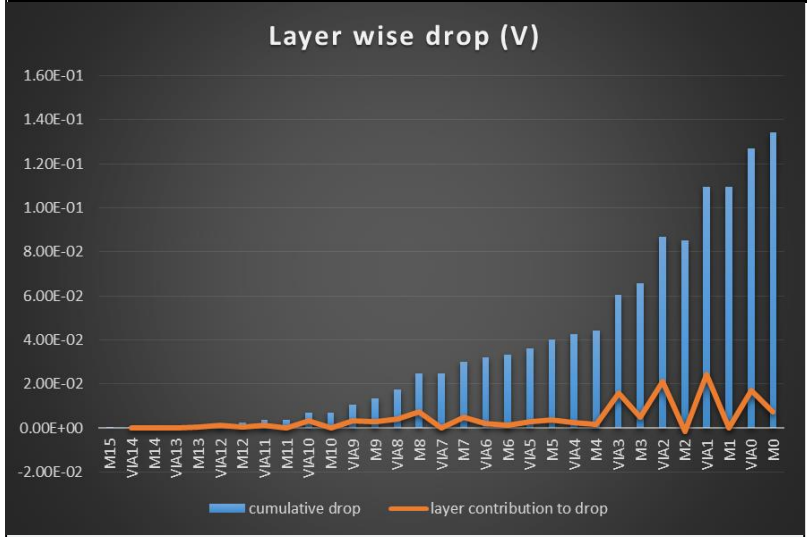
- Replaced adjacent dual M1 same net straps by M1 staples of power and ground staples (VIA stack).
- Staples on M1, M2, M6, M7, M10 and M11



- M1 same-net pitch is half of baseline option– reduced M0 tapping distance by half

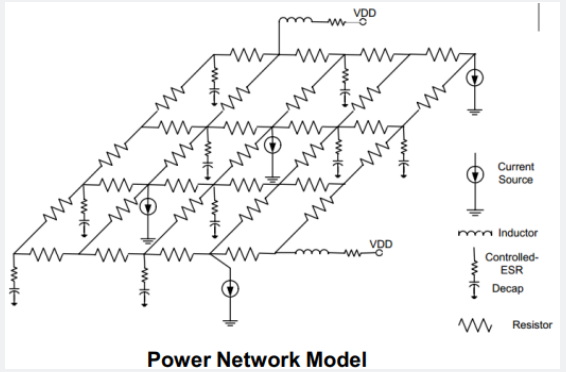
IR drop analysis summary

Parameters	Option-1
IR drop and EM analysis Runs	
Average Power (mW)	361.78
Worst Static IR drop (% of Nom voltage)	3.02
IR drop violation count (threshold 3%)	20
Worst Dynamic IR (% of Nom voltage)	16.53
Dynamic IR violation count (thres. -10%)	801
PG decap (pF)	18.772

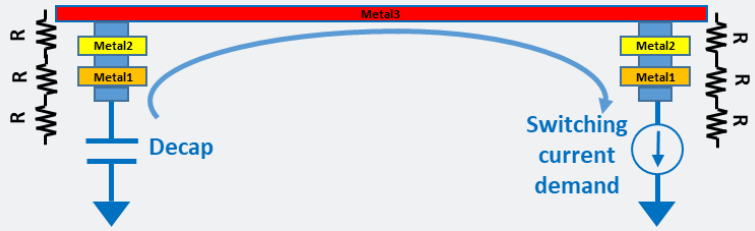


- M0 IR drop contribution down by half
- reduced top layer IR drop contribution
- VIA3 to VIA0 major IR drop contributors

- Lower static IR drop but higher dynamic drop than baseline option



Power Network Model



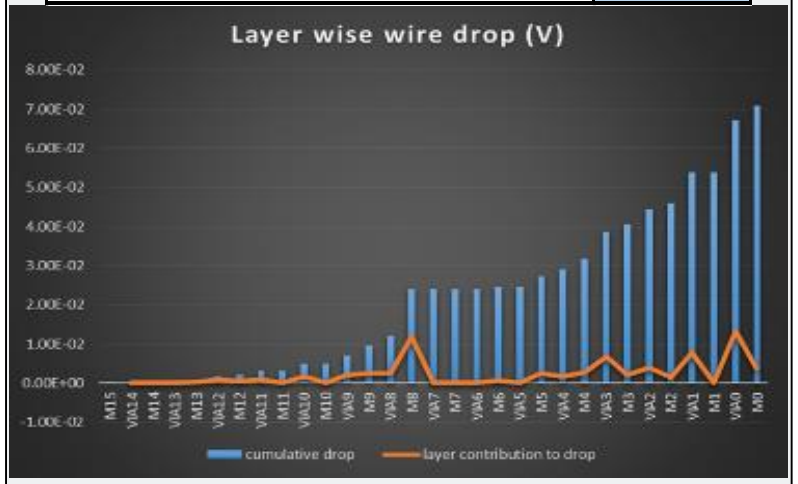
- Staples or VIA ladder on M1 and M2 resulting in high ohmic connection to local decap fabric

PG Grid Evaluations - Option2/3/4 Grid

Option2 Strategy and IR drop summary :

- continuous M1/M2 grid, staples on M6, M7, M10 and M11
- M3 pitch reduced slightly

Parameters	Option-2
IR drop analysis Runs	
Average Power (mW)	357.77
Worst Static IR drop (% of Nom voltage)	2.64
IR drop violation count (threshold 3%)	0
Worst Dynamic IR (% of Nom voltage)	13.05
Dynamic IR violation count (thres. -10%)	85
PG decap (pF)	31.391

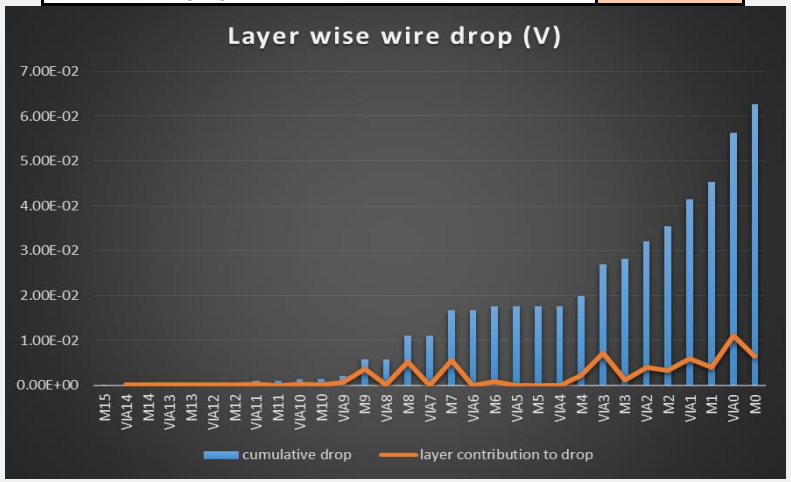


- Continuous M1/M2 helps charge sharing

Option3 Strategy and IR drop summary :

- All layers continuous grid
- Slight reduction in M3 pitch

Parameters	Option-3
IR drop analysis Runs	
Average Power (mW)	365.8
Worst Static IR drop (% of Nom voltage)	2.21
IR drop violation count (threshold 3%)	0
Worst Dynamic IR (% of Nom voltage)	8.59
Dynamic IR violation count (thres. -10%)	0
PG decap (pF)	49.376

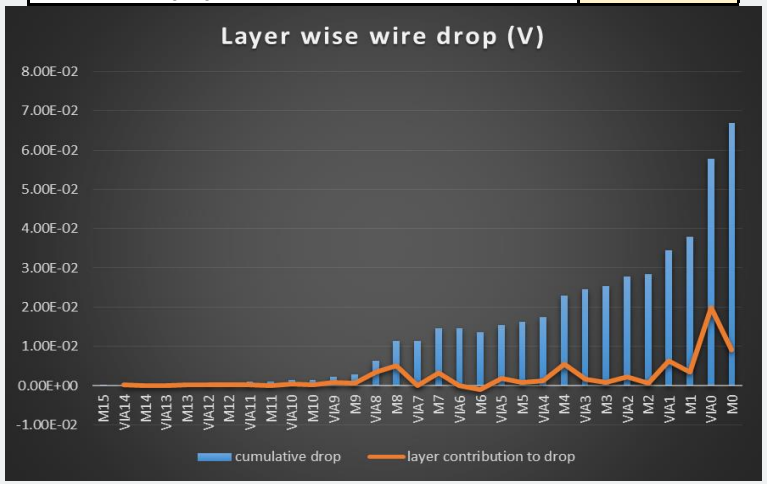


- Significant reduction in dynamic IR drop

Option 4 strategy and IR drop summary:

- overdesigned grid
- Doubled M2 PG density from option3

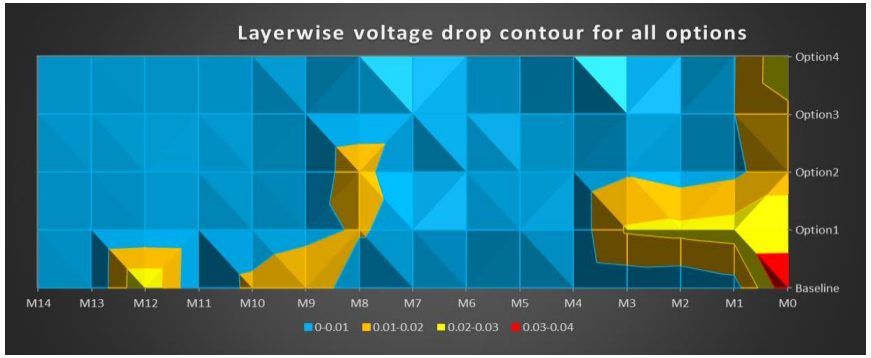
Parameters	Option-4
IR drop analysis Runs	
Average Power (mW)	381.17
Worst Static IR drop (% of Nom voltage)	1.59
IR drop violation count (threshold 3%)	0
Worst Dynamic IR (% of Nom voltage)	9.82
Dynamic IR violation count (thres. -10%)	0
PG decap (pF)	84.793



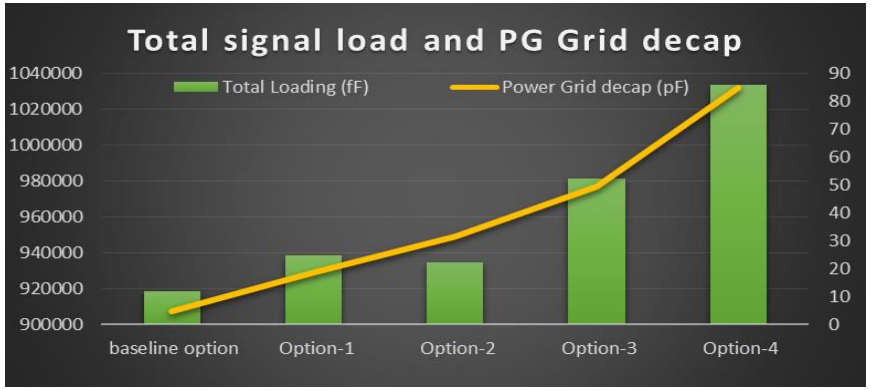
- Reduction in static IR drop but increase dynamic drop

Analysis Results

Proposed methodology based PG provides balanced voltage drop contour across all layers compared to any other options



Parameters	Baseline option	Option-1	Option-2	Option-3	Option-4
Place and Route Run					
DRC count	731	8	16	3	12
Shorts count	125	0	0	0	0
Average Loading (fF)	1.57786	1.6086	1.62204	1.74028	1.87759
Peak (max) Loading (fF)	198.3168	202.25	214.9617	229.4606	236.771
Total Loading (fF)	918332	938310	934272	981445	1033229
Router runtime (Hours)	8.87	14.01	7.47	9.15	10.36
Average Power (mW)	354.14	361.78	357.77	365.8	381.17



Baseline Grid :

1. High DRC/shorts count – M2 overhangs blocking pin access and key layer to switch to higher layers.
2. Maximum routing resources available - Lowest signal loading, average power and router runtime
3. Inadequate IR drop performance

Option1 Grid (M1 and M2 via pillars):

1. High route times – jogs around many tiny M1/M2 DP geometries
2. Higher dynamic IR drop due to increased resistance to local decap fabric
3. Higher signal loading and power than baseline option
4. Lower DRC count - M1/M2 via placement avoiding signal pin blocking

Option2 Grid (M1 and M2 continuous):

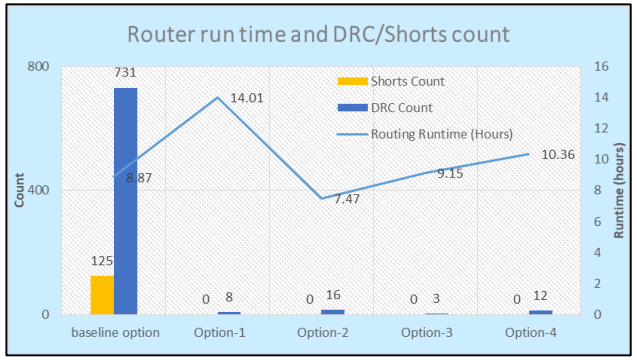
1. Lower runtime and DRCs - improved pin access & continuous grid on DP layers
2. Lower average signal loading and average power than option1
3. Significantly lower dynamic IR - low impedance to decap fabric

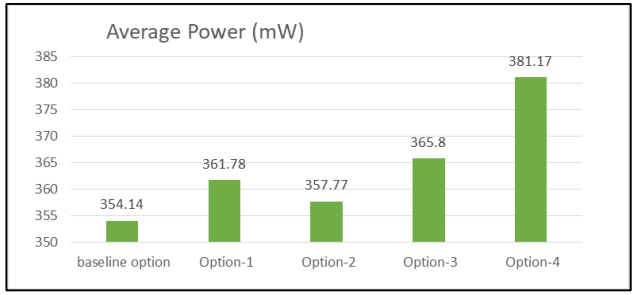
Option3 Grid (continuous grid on all layers):

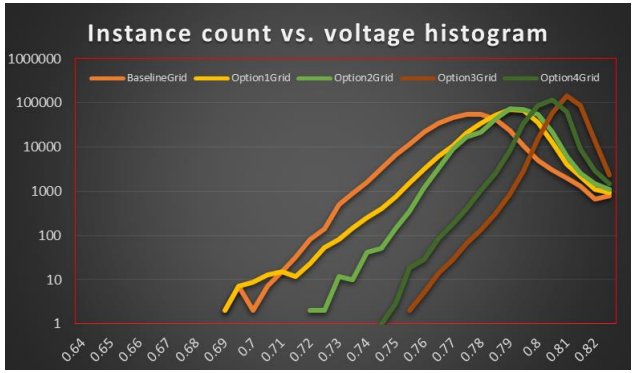
1. Increased signal load and power due to lower resources available, DRCs in control
2. Very good dynamic IR –

Option4 Grid (overdesigned grid):

1. Significant increase in signal loading, average power & router runtime
2. Dynamic IR drop impacted to increased loading and power density

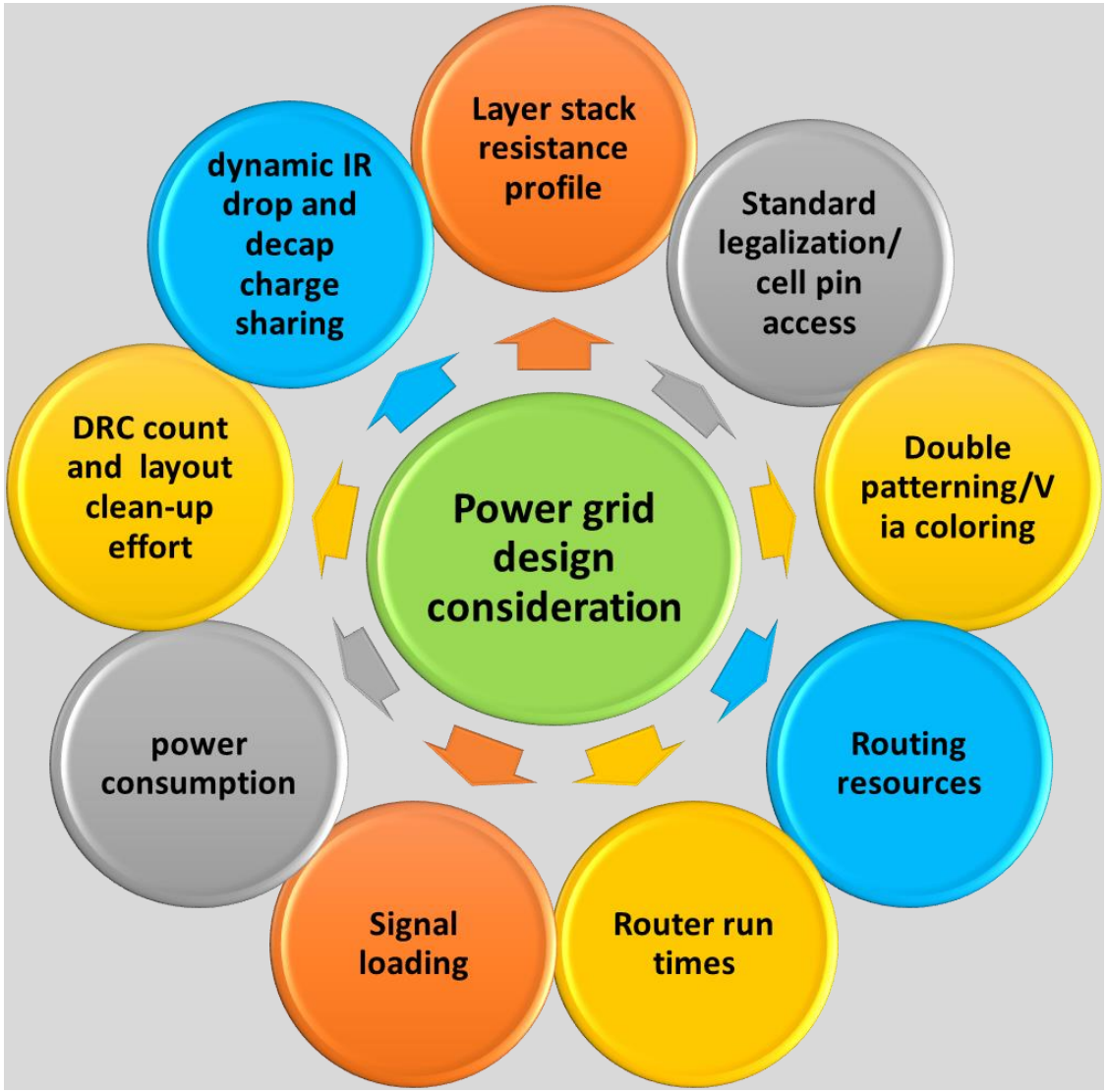






Conclusion : Option3 offers right tradeoff with best IR drop performance and routability with reasonable compromise on runtime and power.

Conclusion : Power Grid Design Impinging Issues



While the primary objective of power grid is to reliably supply required voltage and current to the logic cells, it should conform to below considerations

- Standard cell architecture, Double patterning and coloring rules
- Global vs Local power grid approach and charge sharing
  - Global power grid should provide low resistance connection to the switching logic
  - Local power grid should help during dynamic switching
- Pillared grid doesn't always provide more signal routing resources
- Shouldn't be overdesign :
  - impacts available signal routing resources and increase DRC count and LV clean up effort as well as router run times
  - Higher Signal loading and thereby total power consumption

Power grid design in lower technology nodes is becoming extremely complex and challenging due to stringent technology manufacturing rules and increase in power density. As a result, power grid design must be done carefully considering all the above aspects.

References

- Physical Design Challenges and Innovations to Meet Power, Speed, and Area Scaling Trend, LC LU, TSMC Fellow/Senior Director (R&D), ISPD 2017